

The diagram illustrates a system architecture for three private PC microcomputers (A, B, and C) connected to a terminal. The system is divided into three main sections, each corresponding to one of the private PC microcomputers.

- Private PC Microcomputer Section (Top):** Each private PC microcomputer (4A, 4B, 4C) contains a **DECIPHERING UNIT FOR PRIVATE COMPUTER**. These units are connected to a common bus (24) via switches (SW1, SW2, SW3) and relays (a1, a2, a3).
- Enciphering Unit for Terminal Section (Middle):** Each private PC microcomputer is connected to an **ENCIPHERING UNIT FOR TERMINAL** (23) via a switch (b1, b2, b3) and a relay (24).
- Terminal Section (Bottom):** Each enciphering unit is connected to a **DETECTING UNIT** (21) via a switch (c1, c2, c3) and a relay (24).
- Terminal Connections:** The detecting units are connected to terminals A, B, and C (KB-1, KB-2, KB-3) via switches (d1, d2, d3) and relays (24).

The diagram shows a complex interconnection of switches and relays, indicating a flexible routing mechanism for data between the private PC microcomputers, the terminal enciphering units, and the terminal detecting units.

Fig.1b

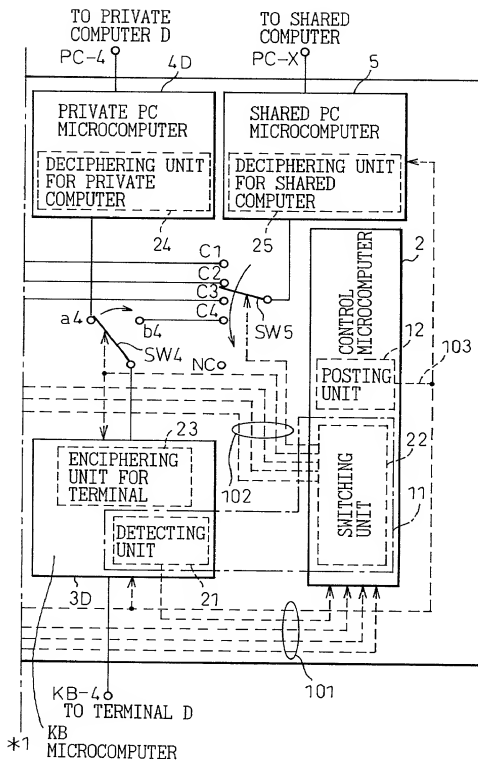


Fig.2a

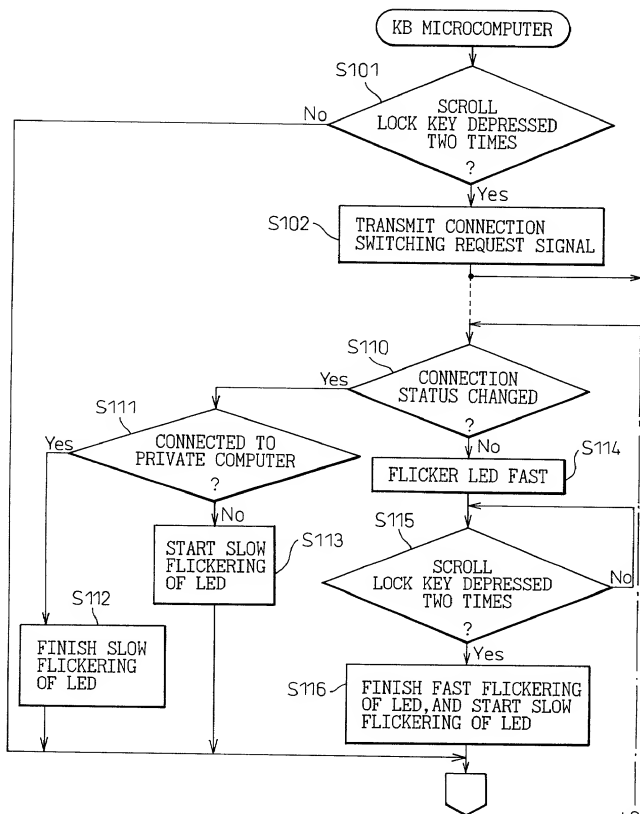


Fig.2b

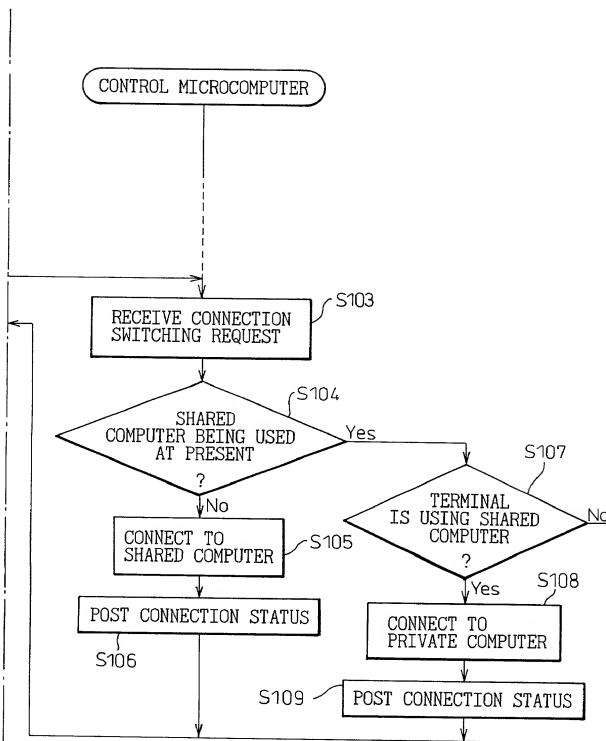


Fig.3

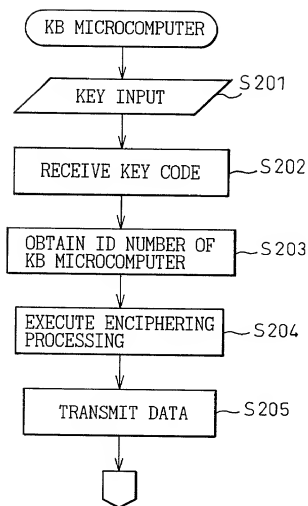


Fig. 4

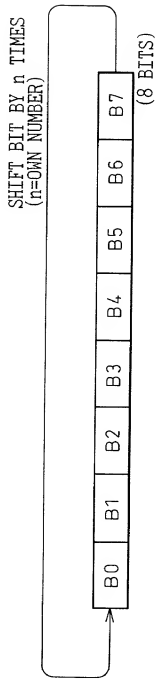
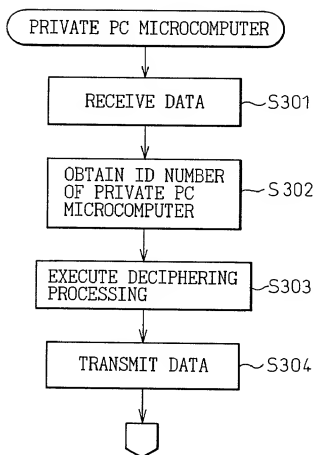


Fig.5



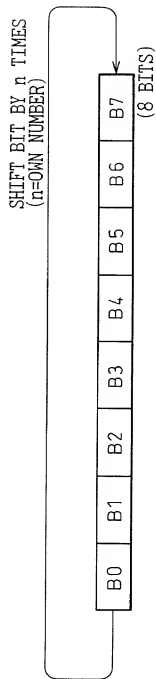


Fig. 6

Fig. 7

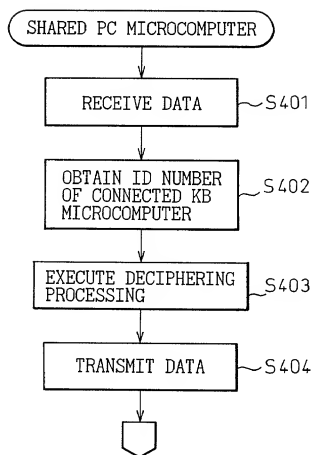


Fig. 8

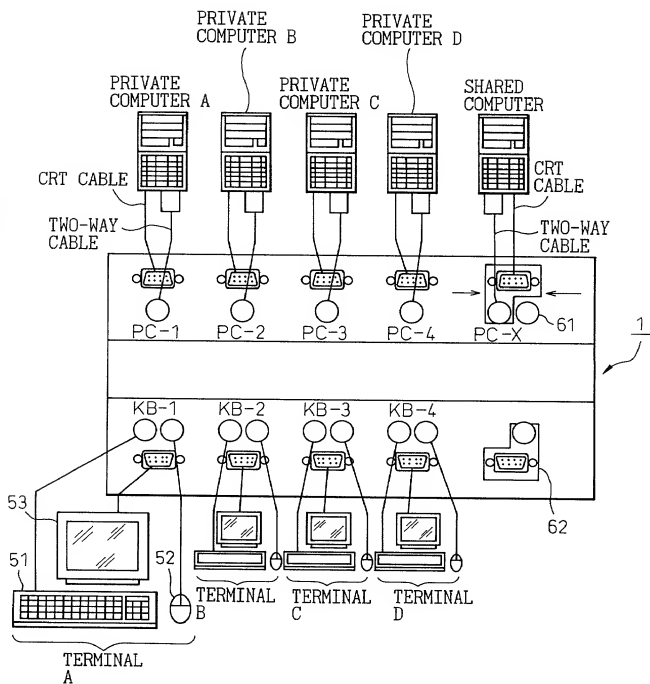


Fig. 9

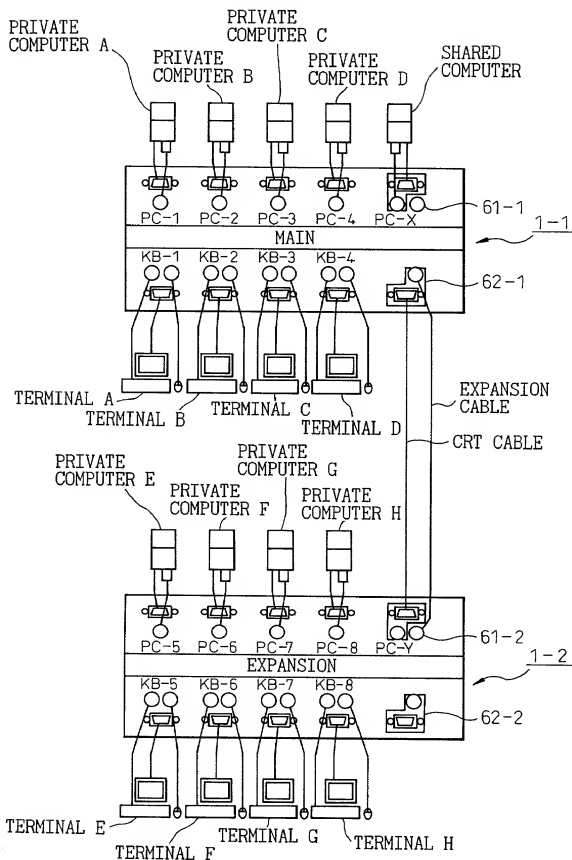


Fig.10

